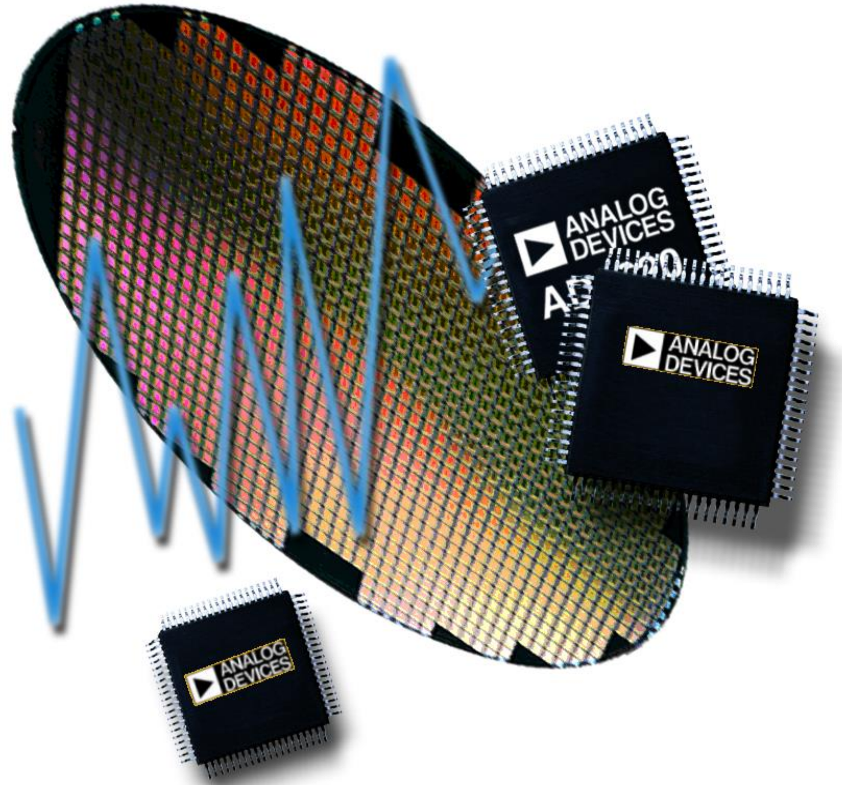

Reliability Report

Report Title: ADM1266 in LFCSP at UT2 Qualification

Report Number: 18024

Revision: A

Date: 8 December 2021

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the ADM1266 product in a 64-LFCSP package at UTAC Thailand (UT2). The ADM1266 is a Cascadable Super Sequencer with Margin Control and Fault Recording.

Table 1: ADM1266 Product Characteristics

Die/Fab

Die Id	TMIH86/D	TMIH87/A
Die Size (mm)	3.02 x 4.88	2.28 x 4.01
Wafer Fabrication Site	TSMC Fab-8B	TSMC Fab-3C
Wafer Fabrication Process	0.18um DMOS	0.18um CMOS
Approximate Transistor Count	10,000	10,000
Passivation Layer	undoped-oxide/SiN	undoped-oxide/OxyNitride
Bond Pad Metal Composition	AlCu(0.5%)	AlCu(0.5%)

Package/Assembly

Package	64-LFCSP
Body Size (mm)	9.00 x 9.00 x 0.75
Assembly Location	UTAC Thailand (UT2)
Molding Compound	Sumitomo G770SHC
Die Attach	Ablestik 8200T
Wire Type	Tanaka GMG 4N Gold
Wire Diameter (mils)	1.00
Lead Frame Material	Copper
Lead Finish	100Sn
Moisture Sensitivity Level	3
Maximum Peak Reflow Temperature	260°C

Description / Results of Tests Performed

Tables 2 through 4 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: LFCSP at UTAC Thailand (UT2) Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADM1266	Q18024.1.HS1	32	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [1]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	ADM1266	Q18024.1.HA4	32	0
				Q18024.2.HA2	32	0
				Q18024.3.HA3	32	0
Solder Heat Resistance (SHR) [1]	J-STD-020	MSL-3	ADM1266	Q18024.1.SH1	11	0
				Q18024.2.SH2	11	0
				Q18024.3.SH3	11	0
Temperature Cycling (TC) [1]	JESD22-A104	-65°C/+150°C, 500 Cycles	ADM1266	Q18024.1.TC1	32	0
				Q18024.2.TC2	32	0
				Q18024.3.TC3	32	0
Unbiased HAST (UHST) [1]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	ADM1266	Q18024.1.UH1	32	0
				Q18024.2.UH2	32	0
				Q18024.3.UH3	32	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Table 3: 0.18µm CMOS FLASH at TSMC Fab-3C Fab Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Data Retention Bake	JESD22-A117	150°C, 1,000 Hours	AD7166	Q11606.15	45	0
				Q11606.16	45	0
Data Retention Bake[1]	JESD22-A117	150°C, 1,000 Hours	AD81005	Q11794.HT1	77	0
				Q11794.HT3	77	0
Data Retention Bake[1]	JESD22-A117	150°C, 1,000 Hours	AD7166	Q9855.2	77	0
				Q9855.4	77	0
			ADUCM362	Q11483.DR1	77	0
				Q11483.DR2	77	0
				Q11483.DR3	77	0
Early Life Failure Rate (ELFR)	MIL-STD883, M1015	125°C, 48 Hours	ADUCM350	Q10082.16	105	0
				Q10082.17	200	0
				Q10082.18	200	0
				Q10082.19	162	0
				Q10082.20	70	0
				Q10082.21	200	0
				Q10082.22	200	0
				Q10082.23	200	0
				Q10082.24	70	0
				Q10082.25	200	0
				Q10082.26	200	0
				Q10082.27	200	0
			AD7160	Q7981.56	85	0
				Q7981.57	85	0
				Q7981.58	85	0
				Q7981.59	84	0
				Q7981.60	85	0
				Q7981.61	85	0
				Q7981.62	85	0
				Q7981.63	83	0
				Q7981.64	85	0
				Q7981.65	85	0
				Q7981.66	85	0
				Q7981.67	85	0
				Q7981.68	85	0
				Q7981.69	85	0
				Q7981.70	85	0
				Q7981.71	85	0
				Q7981.72	85	0
				Q7981.73	85	0
				Q7981.74	85	0
				Q7981.75	77	0
				Q7981.76	85	0
				Q7981.77	85	0
				Q7981.78	85	0
				Q7981.79	87	0

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
EEPROM Endurance Cycling	JESD22-A117	-40°C, 20K Cycles, Single Duration	ADUCM350	Q10175.10	32	0
		-40°C, cycles to failure, Single Duration	AD7166	Q11606.12	32	0
				Q11606.13	45	0
				Q11606.14	45	0
		125C, 20K Cycles, Single Duration	ADUCM350	Q10175.12	32	0
		25C, 20K Cycles, Single Duration		Q10175.11	32	0
		85C, 10K Cycles, Single Duration	AD7166	Q11606.2	77	0
		85C, cycles to failure, Single Duration	AD7166	Q11606.10	45	0
				Q11606.11	45	0
				Q11606.17	45	0
				Q11606.9	45	0
EEPROM Endurance Cycling[1]	JESD22-A117	85C, 10K Cycles, Single Duration	AD81005	Q11794.END3	77	0
EEPROM Endurance Cycling[2]	JESD22-A117	-40°C, 10K Cycles, Single Duration	ADUCM362	Q11483.EC3	77	0
		-40°C, 20K Cycles, Single Duration	ADUCM350	Q10082.14	32	0
		125C, 10K Cycles, Single Duration	ADUCM362	Q11483.EC2	77	0
		25C, 20K Cycles, Single Duration	ADUCM350	Q10082.3	32	0
High Temperature Operating Life (HTOL)	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	AD7161	Q9146.13	77	0
				Q9146.3	77	0
				Q9146.5	77	0
			AD7166	Q9855.1	77	0
			AD81005	Q11794.HO1	77	0
				Q11794.HO2	77	0
				Q11794.HO3	77	0
				Q11794.HO4	77	0
			ADUCM360	Q8874.11	77	0
				Q8874.20	77	0
				Q8874.4	77	0
		125°C<Tj<135°C, Biased, 500 Hours	AD7166	Q11606.6	45	0
		125°C<Tj<135°C, Biased, P2500	ADuCRF02	Q8248.2	45	0
				Q8248.4	32	0
				Q8248.6	45	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	AD7166	Q9408.4	45	0
			ADM1266	Q11688.13	32	0

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
				Q11688.32	32	0
				Q18024.1.HS1	32	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [2]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	AD7160	Q7981.42	77	0
				Q7981.46	77	0
			ADUCM350	Q10082.12	32	0
				Q10082.2	32	0
				Q10175.2	32	0
			ADUCM360	Q8874.1	77	0
				Q8874.18	77	0
				Q8874.6	77	0
				Q8874.7	77	0
			ADM1266	Q18024.1.HA4	45	0
				Q18024.2.HA2	32	0
				Q18024.3.HA3	32	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 168 hrs @ 85°C, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

[2] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Table 4: 0.18um DMOS at TSMC Fab-8B
Fab Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)	MIL-STD883, M1015	125°C, 48 Hours	ADUCM4135	Q11117.22	500	0
				Q11117.31	500	0
				Q11117.32	500	0
				Q11117.33	307	0
				Q11117.34	300	0
				Q11117.35	300	0
			SSM3582	Q11336.EL1a	85	0
				Q11336.EL1b	85	0
				Q11336.EL1c	85	0
				Q11336.EL1d	84	0
				Q11336.EL2	85	0
				Q11336.EL2a	85	0
				Q11336.EL2b	85	0
				Q11336.EL2c	83	0
				Q11336.EL2d	85	0
				Q11336.EL3	85	0
				Q11336.EL3a	85	0
				Q11336.EL3b	85	0
				Q11336.EL3c	85	0
				Q11336.EL3d	200	0
High Temperature Operating Life (HTOL)	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	AD2410W	QL10667HTL01	77	0
				QL10667HTL03	77	0
			ADuM4135	Q11117.1	77	0
				Q11117.7	77	0
				Q11117.8	77	0
			SSM3515	Q12089.10	77	0
				Q12089.5	77	0
			SSM3582	Q11336.HO2	77	0
				Q11336.HO3	77	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADM1266	Q11688.13	32	0
				Q11688.32	32	0
				Q13288.4	32	0
				Q18024.1.HS1	32	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [1]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	AD2410W	Q7981.42	77	0
				Q7981.46	77	0
			ADXRS290	Q10082.12	32	0
				Q10082.2	32	0
				Q10175.2	32	0
			ADM1266	Q18024.1.HA4	45	0
				Q18024.2.HA2	32	0
				Q18024.3.HA3	32	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

ESD Test Results

The results of Field-Induced Charged Device Model (FICDM) ESD testing is summarized in Table 5. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on Analog Devices' web site).

Table 5: ADM1266 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	64-LFCSP	JS-002	1Ω, Cpkg	±750V	±1000V	C2b
HBM	64-LFCSP	ESDA/JEDEC JS-001-2011	1.5kΩ, 100pF	±2000V	±2500	2
MM	64-LFCSP	JESD22-A115	0Ω, 200pF	±200V	±400V	N/A

Latch-Up Test Results

Three samples of the ADM1266 were latch-up tested at TA=25°C per JEDEC Standard JESD78, Class I, as per QP#13745. All pins passed.

Passing positive current	Passing negative current	Passing Over-Voltage
+ 100 mA	- 100 mA	+22.5 V

- 100Ω series resistance used when testing pins 2 and 3

Approvals

Reliability Engineer: Arvin Jay Escolano

Additional Information

Data sheets and other additional information are available on Analog Devices' web site

PCN 21_0180

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

Feature	ASE (CP-64-15)			UTAC (CP-64-23)			Remarks
	Min	Nom	Max	Min	Nom	Max	
A (Pkg height)	0.70	0.75	0.80	0.70	0.75	0.80	Same
A1 (Stand-off)		0.02	0.05		0.02	0.05	Same
A3 (LF thickness)	0.203 REF			0.203 REF			Same
D (Body width)	8.90	9.00	9.10	8.90	9.00	9.10	Same
E (Body length)	8.90	9.00	9.10	8.90	9.00	9.10	Same
D2 (Exposed pad width)	7.50	**7.60**	7.70	7.40	**7.50**	7.60	New site UT2 exposed pad size is smaller
E2 (Exposed pad length)	7.50	**7.60**	7.70	7.40	**7.50**	7.60	New site UT2 exposed pad size is smaller
b (Lead width)	0.18	0.25	0.30	0.20	0.25	0.30	same nominal value
e (Lead pitch)	0.50 BSC			0.50 BSC			same
L (Lead length)	0.35	0.40	0.45	0.30	0.40	0.50	same nominal value